EL ENG 143: Microfabrication Technology

Lab Report 1: NMOS Microfabrication Process

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UC Berkeley, Department of Electrical Engineering and Computer Science
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Wednesday 2PM-5PM: Group 21
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Fall 2025

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Contributions

In this section, we list how each member contributed to each section of the report.

- **Larry** edited the abstract, did the general formatting and typesetting in LaTeX, performed theoretical calculations for oxide thickness and to determine the distribution of dopants vs. wafer depth in the N-doped areas of the final wafer, and helped with the potpourri of microfabrication processes questions in section.
- **Arhaan** calculated the overetching lengths, recorded the process parameters in the tables, and helped with the potpourri of microfabrication processes questions in section.
- **Emerson** recorded the pictures from the microscope, drew all figures and wrote descriptions for all the fabrication steps, measured the overetching lengths in J-Image, wrote the abstract, and helped with the potpourri of microfabrication processes questions in section.

All authors reviewed the final manuscript.

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PART 1: Summary and Course Feedback

1 Abstract and Feedback

This lab report was completed as a requirement for EL ENG 143 at the University of California, Berkeley. It is the first required lab report and outlines the step-by-step fabrication process of a $\langle 100 \rangle$ silicon wafer containing several learning integrated circuits (ICs). Specifically, we fabricated MOSFETs, ring oscillators, comb drives, cantilever arrays, and a heater platform on our wafer. In making these components, we learned to carry out major microfabrication techniques with precision. Our production sequence consisted of nine steps: field oxidation, active-area photolithography and etching, gate oxidation, polysilicon deposition, gate photolithography and etching, source and drain doping, dopant drive-in and intermediate oxidation, contact-hole photolithography, metallization, and metallization photolithography and etching. These steps form the foundation of modern chip manufacturing, and learning them was both rewarding and enjoyable.

Dry and wet oxidation were used to form insulating layers, and successive photolithography steps patterned the active devices, gate regions, contact openings, and metal routing. A combination of wet and dry etching sculpted the film geometries, followed by thermal evaporation to deposit the aluminum metallization. After each major step, we characterized oxide thickness, sheet resistance, and mask alignment to track how the fabrication sequence altered the wafer. The process demonstrated good fidelity, with only minor over-etching and slight misalignments. During the photolithography steps, there were instances where we had to re-apply photoresist when the coating did not spread evenly. Mask alignment was also not perfect, though we did our best to minimize errors.

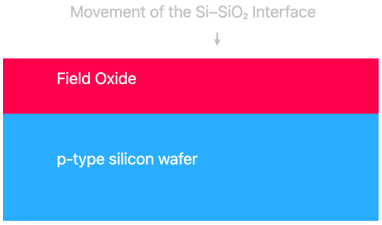
Overall, the workflow proceeded smoothly: the same wafer was used from start to finish without shattering, the critical dimensions were met, and the resulting electrical behavior aligned well with expectations. Most deviations remained below 10%, indicating negligible impact from our handling. We learned that microfabrication demands both precision and patience. Tuning the HF etch time required experimentation since we had no means of in-situ monitoring, but ultimately produced satisfactory results when etching the field oxide. Under Carolyn's guidance, this lab provided a rare and valuable hands-on immersion into NMOS fabrication and culminated in the production of a fully functional device wafer.

PART 2: Experimental Process and Details

2.1 Major Fabrication Steps

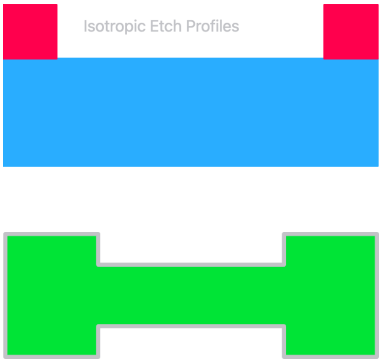
1. Field Oxidation (done by TAs)

   Field oxidation is grown by the TAs in the Nanolab. Silicon dioxide is grown from silicon with wet oxidation in a Tystar 2 furnace. We grow field oxide on the silicon wafer base to keep components that we will eventually create to be insulated from each other, since silicon dioxide is an excellent insulator.



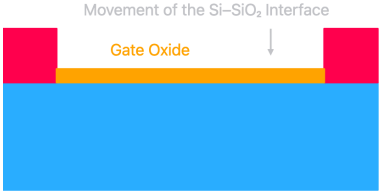
2. Active Area (ACTV) Photolithography & Etch

   The active area is created by etching away the field oxide to expose a working area of the underlying silicon, where components can be built upon. The wafer is first coated with positive photoresist. Then, ultraviolet light shines through a photomask to weaken exposed photoresist. The weakened photoresist is then removed and the exposed silicon dioxide is removed. We need this step because otherwise the wafer will just be coated in silicon dioxide, which alone is an insulator.



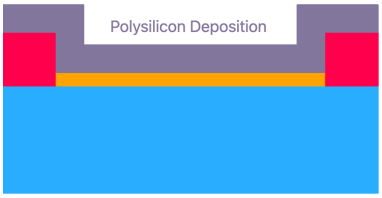
3. Gate Oxidation

   In the gate oxidation step, we grow a thin layer of silicon dioxide from the exposed silicon in the exposed active area. The gate oxide is needed to form an insulating layer between the gate and the underlying silicon, which will contain the source and the drain.



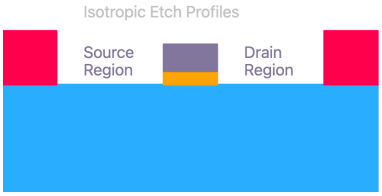
4. Polysilicon Deposition (done by TAs)

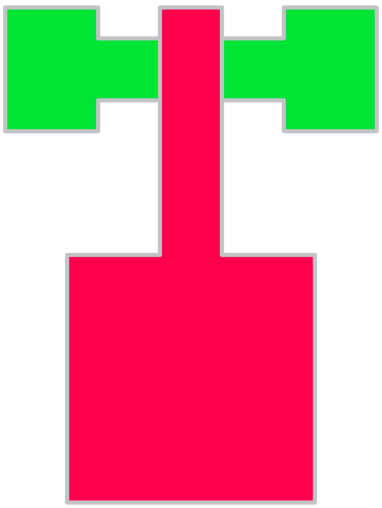
   Polysilicon deposition is done by TAs in the Tystar10 furnace. Silane is used to supply silicon and phosphorus so we grow a slightly n-doped polysilicon layer. The polysilicon deposition step is needed to deposit the silicon layer required to form the gate of the MOSFET.



5. Gate (POLY) Photolithography & Etch

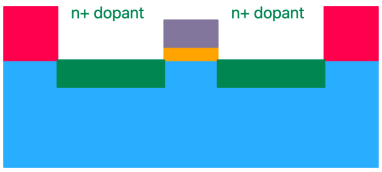
   The gate photolithography & etch step creates the source and drain regions on the silicon wafer by etching the gate oxide. The MOSFET is also formed by the remaining polysilicon. This step is performed with the standard lithography procedure described in step 2, with the exception that this step uses the POLY mask on the lithography machine.





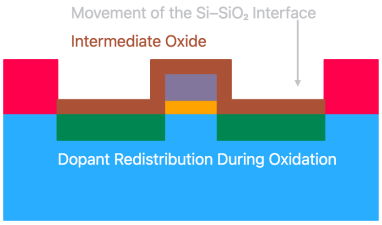
6. Source/Drain Doping

   The source/drain doping step creates the n+ dopant regions on the exposed silicon wafer for the MOSFET source and drains This is performed by first coating the wafer with spin-on dopant, then baking the wafer to remove solvent, then diffusing the dopant via the 1050 °C furnace. This step is necessary because the n+ source and drain regions are where external wires will connect to, forming the source and gates of the MOSFET.



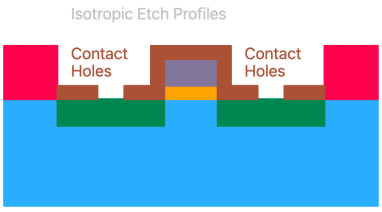
7. Dopant Drive-in & Intermediate Oxidation

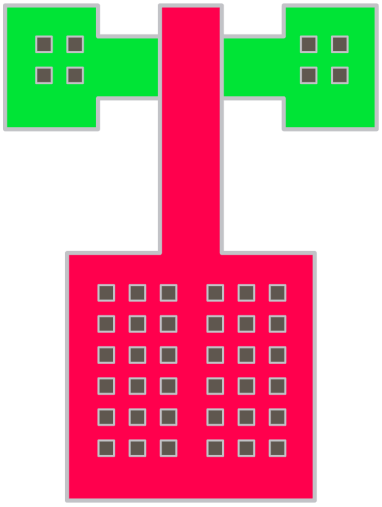
The dopant drive-in and intermediate oxidation steps aim to grow a layer of intermediate oxide around the source and drains to act as insulation for their metal connectors. This step is performed by growing silicon oxide with wet oxidation, because it grows oxide faster.



8. Contact Hole (CONT) Photolithography & Etch

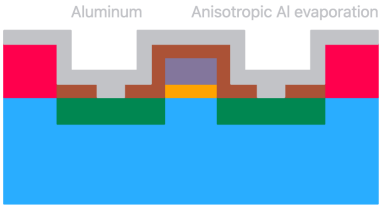
The contact hole photolithography and etch step etches a contact hole in the intermediate oxide for the metal connectors to form, which allows the n+ doped source and drain regions to the surface via a conducting connector. This step is performed with the standard lithography steps with the CONT mask.





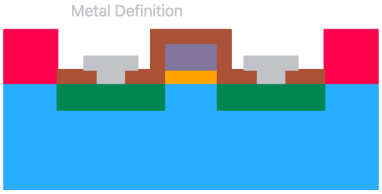
9. Metallization

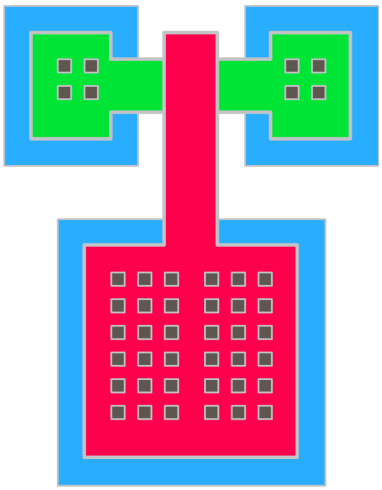
The metallization step performs physical vapor deposition to deposit a layer of aluminum across the entire wafer. This step is performed specifically to form metal contacts between the source and drain regions and the surface of the wafer. We deposit aluminum across the entire wafer first before etching the metal layer.



10. Metal (METL) Photolithography & Etch

    The metal photolithography and etch steps etches the deposited aluminum to form aluminum contacts only at the regions right above the n+ source and drain regions, insulated by the intermediate oxide. This step is necessary because otherwise the aluminum layer will conduct electricity directly between the source and drain regions if it is not etched away. This step is performed with the standard lithography steps with the METL mask.





    The tables below summarize all of the important parameters and their corresponding values for each major fabrication step. Photos are included for the active lithography, polysilicon, contact lithography, and metallization. These photos are analyzed both post-developed and post-etched to determine if any overetching occured.

2.2 Table of Values and Microscope Pictures

The following are are table of values from each major fabrication step and microscope pictures for each etching step.

Initial wafer + field oxidation

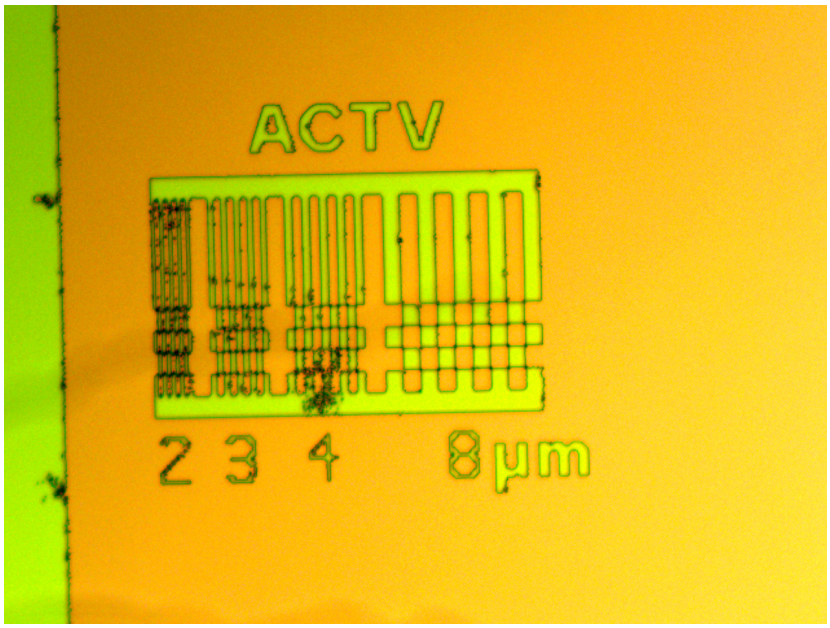
Parameter	Value
Wafer orientation	<1,0,0>
Type of dopant (atom and n-type vs p-type)	Boron p-type
Field oxidation temperature (°C)	1100 °C
Field oxidation time (minutes)	5 min dry oxidation O_2 125 min wet oxidation H_2O 5 min dry oxidation O_2
Field oxidation type (wet or dry)	Dry, then wet, then dry
Measured field oxide thickness (nm)	620 nm
Measured sheet resistance (Ω/square)	296 Ω/square

ACTV photolithography + etch

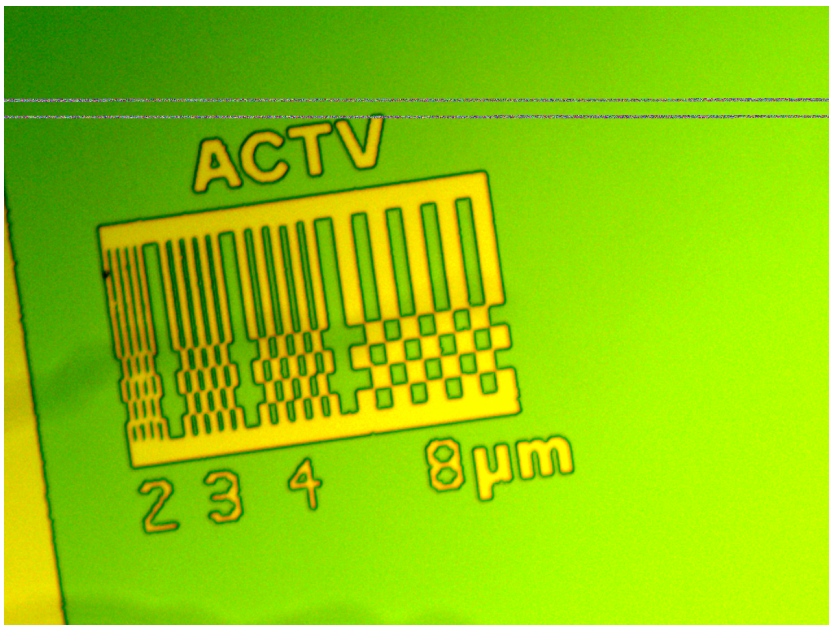
Parameter	Value
Dehydration bake temperature (°C)	110 °C
Dehydration bake time (min)	10 min
HMDS time (min)	5 min
Photoresist spin speed (RPM)	300 rpm
Photoresist spin time (s)	30 s
Soft bake temperature (°C) (on the hot plate)	100 °C
Soft bake time (s)	90 s
Exposure time (s) of the photolithography machine	8 s
Development time (s) to remove photoresist	60 s
Etch time (s) by HF	6min 45 seconds

Overetch (µm)	2 µm	3 µm	4 µm	8 µm	average
After lithography	0.08	0.55	0.57	0.08	0.32
After etch + strip	0.23	0.57	0.59	0.38	0.4425

ACTV Post Develop:



ACTV Post Etch:



Gate oxidation

Parameter	Value
Furnace temperature (°C)	1100 °C
Furnace time (minutes)	50 min then 10 min of N_2 annealing
Oxidation type (wet or dry)	dry
Measured gate oxide thickness (nm)	109.1 nm

Polysilicon deposition

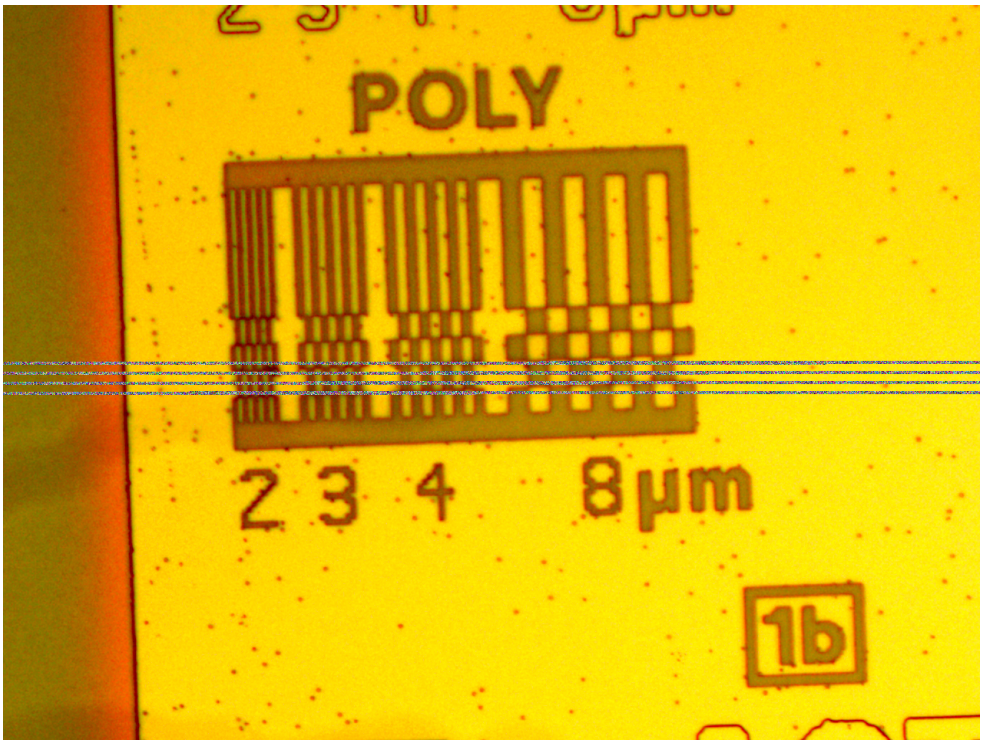
Parameter	Value
Furnace temperature (°C)	650 °C
Furnace time (minutes)	210 min
Measured polysilicon thickness (nm)	500 nm

POLY photolithography + etch

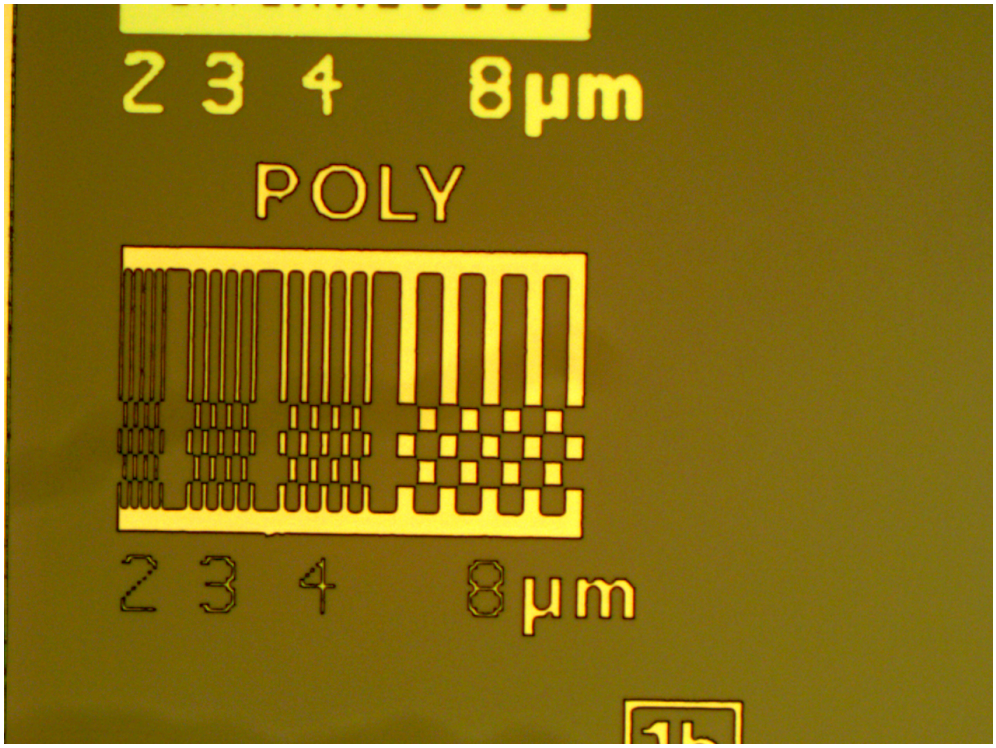
Parameter	Value
Polysilicon etch time (s)	246 s
Gate oxide etch time (s)	180 s

Overetch (µm)	2 µm	3 µm	4 µm	8 µm	average
After lithography	0.22	0.63	0.45	0.89	0.5475
After etch + strip	0.52	0.93	1.63	1.78	1.215

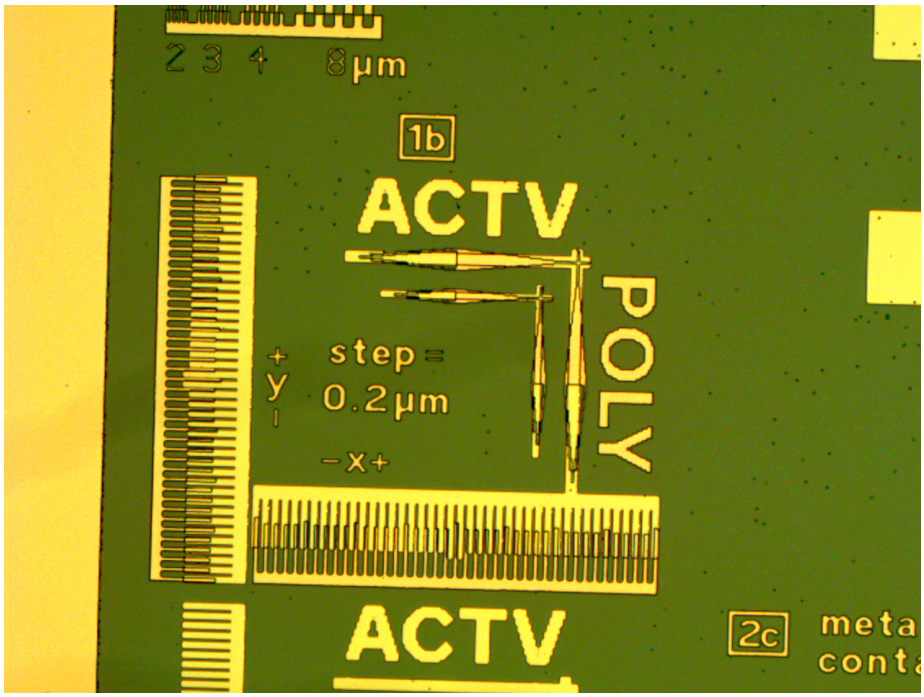
Poly Post Develop:



Poly Post Etch:



ACTV/POLY alignment Mark:



X misalignment (µm)	Y misalignment (µm)
0.039	0.058

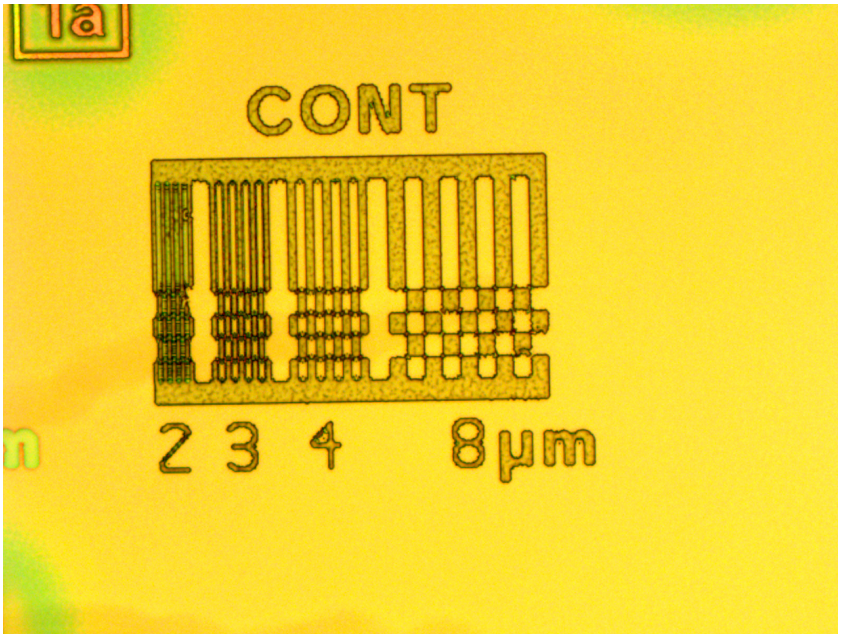
Source/drain doping + intermediate oxidation

Parameter	Value
Doping furnace temperature (°C)	1100 °C
Doping furnace time (min)	5 min
Type of dopant (atom and n-type vs p-type)	n-type
Drive-in furnace temperature (°C)	1100 °C
Drive-in furnace time (min)	20 min
Oxidation type (wet or dry)	Dry Oxidation
Measured intermediate oxide thickness (nm)	67.3 nm
Final control wafer sheet resistance (Ω/square)	5.93 Ω/square

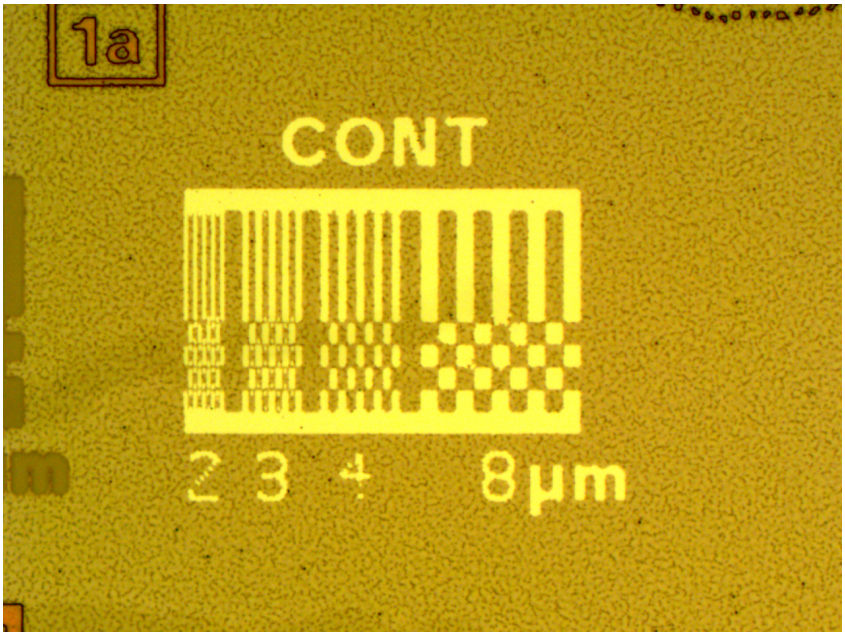
CONT photolithography + etch

Parameter	Value
Oxide etch time (s)	105 s

CONT Post Development:

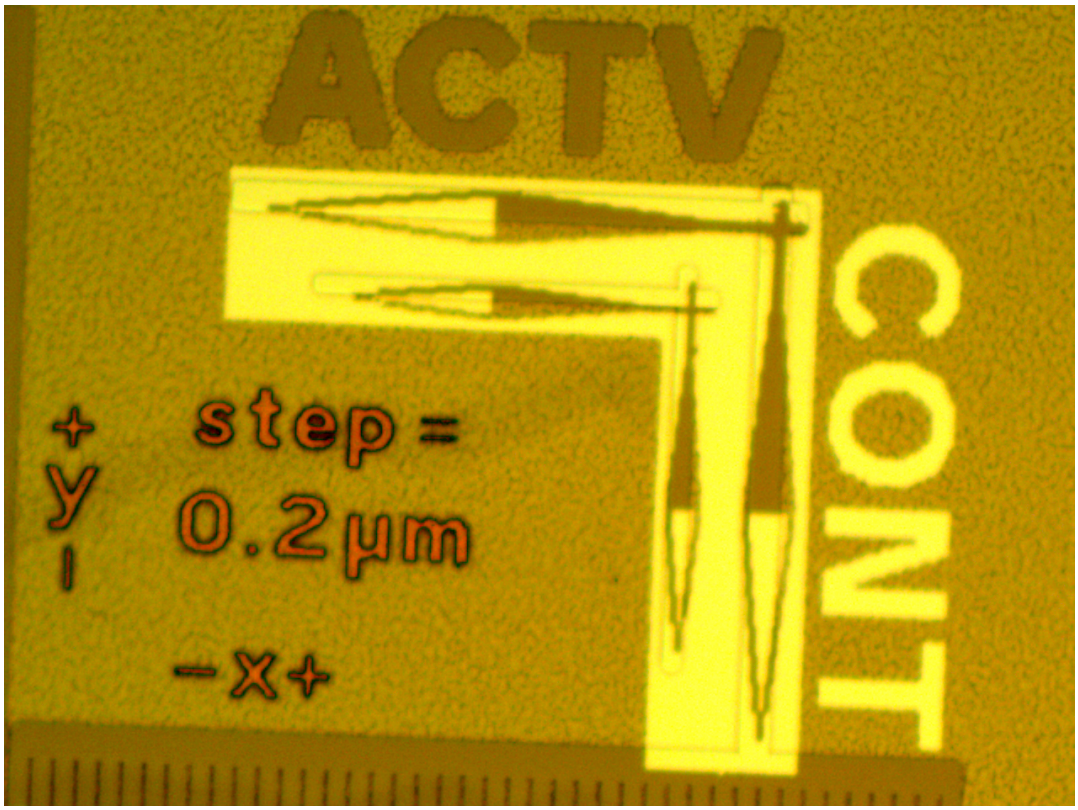


CONT Post strip:



Overetch (µm)	2 µm	3 µm	4 µm	8 µm	average
After lithography	0.23	0.35	0.17	0.33	0.27
After etch + strip	0.53	0.62	1.05	0.33	0.6325

Picture of ACTV/CONT alignment mark



X misalignment (µm)	Y misalignment (µm)
0.058	0.108

No one in our lab section has a picture of the POLY/CONT alignment mark, so Collin advised us to leave a note here instead of going into the lab and taking a picture of the mark.

Metallization

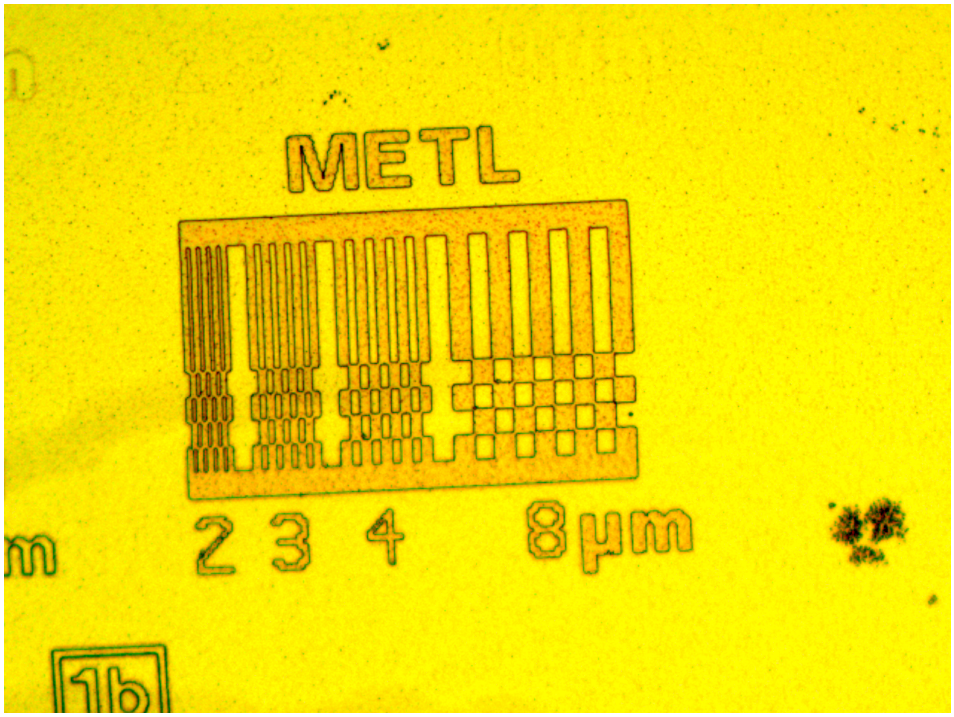
Parameter	Value
Aluminum sheet resistance (Ω/square)	0.12

METL photolithography + etch

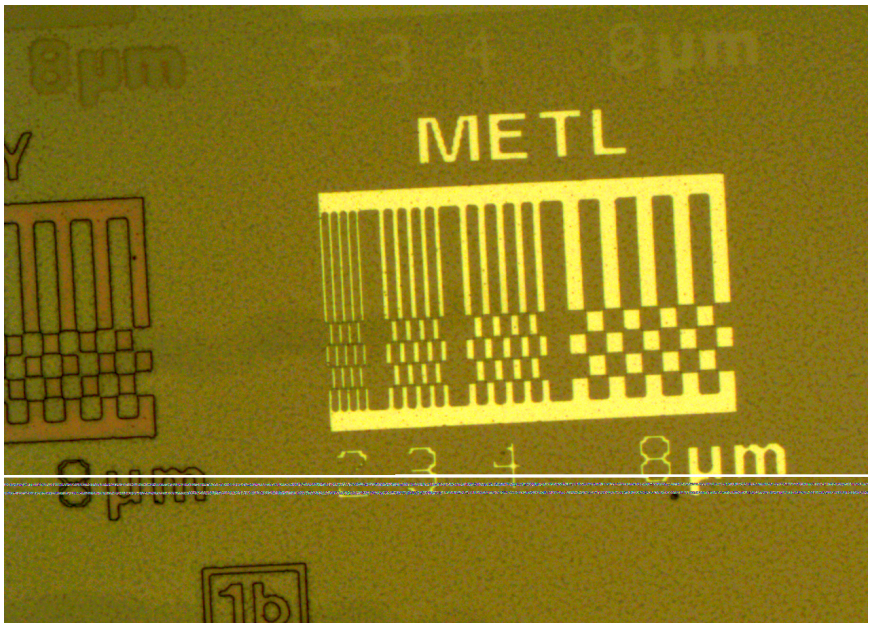
Parameter	Value
Metal etch time (s)	40s
Sintering furnace temperature (°C)	400 ° C
Sintering furnace time (min)	20 min

Overetch (µm)	2 µm	3 µm	4 µm	8 µm	average
After lithography	0.22	0.31	0.43	0.26	0.305
After etch + strip	0.81	0.92	0.73	0.87	0.8325

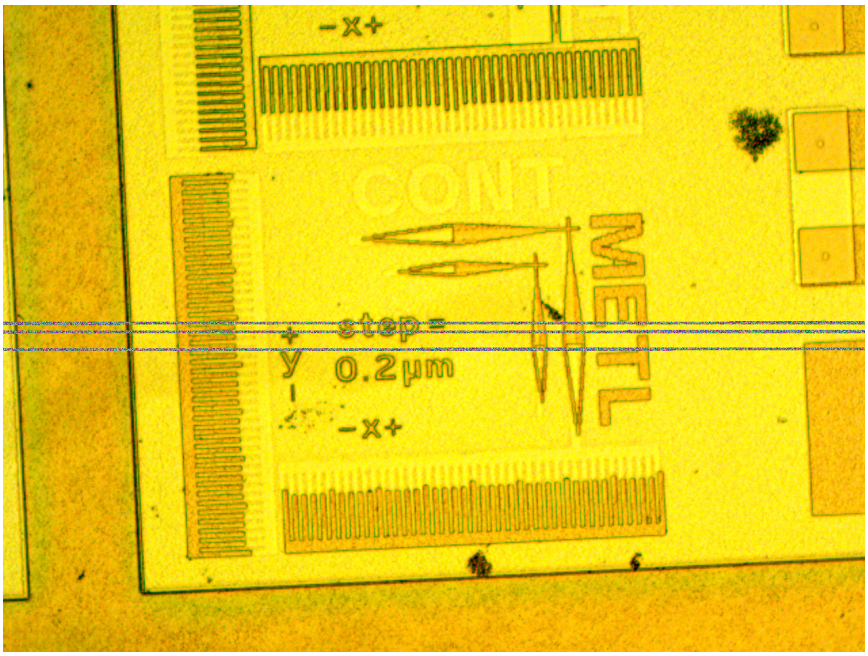
METL Post Develop:



METL Post Etch:



Picture of CONT/METL alignment mark:



X misalignment (μm)	Y misalignment (μm)
0.09	0.02

PART 3: Theoretical Calculations

3.1 Oxide Thicknesses

Assuming that oxygen diffuses through the existing oxide layer, we can use Fick's first law of diffusion. By baking the approximation that the oxygen flux passing through the oxide is constant everywhere in the oxide i.e. oxygen does not accumulate in the oxide, we can simplify our relation to

$$J = -D\frac{\partial N(x,t)}{\partial x} = -D\frac{N_i - N_0}{X_o}$$

where X_o is the thickness of the oxide at a given time, and N_0 and N_i are the concentrations of the oxidizing species in the oxide at the oxide surface and SiO_2 interface respectively. At the SiO_2 interface we assume that the oxidation rate is proportional to the concentration of the oxidizing species so that the flux at the interface is $J = k_s/N_i$, where k_s is the rate constant for the reaction so by eliminating N_i we have

$$J = D\frac{N_0}{X_o + D/k_s}$$

The time derivative of the thickness of the oxide layer is then just the oxidizing flux divided by the number of molecules M of the oxidizing species that are incorporated into a unit volume of the resulting oxide

$$\frac{dX_o}{dt} = \frac{J}{M} = \frac{DN_0/M}{X_o + D/k_2}$$

Employing the boundary condition that X_o at $t = 0$ is X_i, we proceed via separation of variables

$$\frac{dX_o}{dt} = \frac{DN_0/M}{X_o + D/k_2} \implies \left(X_o + \frac{D}{k_s}\right) dX_o = \frac{DN_0}{M}dt$$

Integrating from $t = 0$ where $X_o = X_i$ to an arbitrary time t where $X_o = X_o(t)$

$$\begin{aligned}
\int_{X_i}^{X_o} \left(x + \frac{D}{k_s}\right) &= \int_0^t \frac{DN_0}{M}dt' \\
\frac{X_o^2}{2} - \frac{X_i^2}{2} + \frac{D}{k_s}(X_o - X_i) &= \frac{DN_0}{M}t \\
X_o^2 - X_i^2 + \frac{2D}{k_s}(X_o - X_i) &= \frac{2DN_0}{M}t
\end{aligned}$$

Letting $A \triangleq 2D/k_s$ and $B \triangleq 2DN_0/M$, solving for t and rearranging we have

$$Bt = X_o^2 - X_i^2 + A(X_o - X_i) \implies t = \frac{X_o^2 - X_i^2}{B} + \frac{A}{B}(X_o - X_i) = \left(\frac{X_o^2}{B} + \frac{A}{B}X_o\right) - \left(\frac{X_i^2}{B} + \frac{A}{B}X_i\right)$$

Note that $A/B \equiv 1/(B/A)$ and letting $\tau \triangleq X_i^2/B + X_i/(B/A)$

$$t = \frac{X_o^2}{B} + \frac{X_o}{B/A} - \left(\frac{X_i^2}{B} + \frac{X_i}{B/A}\right) \implies \boxed{t = \frac{X_o^2}{B} + \frac{X_o}{B/A} - \tau}$$

This is the Deal-Grove Model. Using it, we can calculate theoretical thicknesses of the field, gate, and intermediate oxides immediately after they were deposited as follows.

$$X_o^2 + AX_0 = B(t + \tau) \xrightarrow{t=0} X_i^2 + AX_i = B\tau$$

We will assume that the wafer is made with pure $\langle 100 \rangle$ (orientation of oxidation rate) silicon with no initial oxide on the surface so $X_i = 0 \implies X_i^2 = 0 \implies AX_i = 0$ which gives $\tau = 0$. We also know that the ratio B/A is the **linear** rate constant and B is the **parabolic rate constant**. Then the Deal-Grove

constants A and B are related to the temperature, diffusivity, and activation energy of the substrate through an Arrhenius relationship.

$$D = D_{0,p} \exp\left(-\frac{E_{A,p}}{kT}\right),\ k_s = k_{s,l} \exp\left(-\frac{E_{A,l}}{kT}\right)$$

Assuming that N_0 and M are treated as constants because they are weakly temperature-dependent.

$$B = \frac{2N_0}{M} D = \underbrace{\left(\frac{2N_0}{M} D_{0,p}\right)}_{D_{0,p}} \exp\left(-\frac{E_{A,p}}{kT}\right)$$

$$\frac{B}{A} = \frac{k_s N_0}{M} = \underbrace{\left(\frac{N_0}{M} k_{0,l}\right)}_{D_{0,l}} \exp\left(-\frac{E_{A,l}}{kT}\right)$$

These two Arrhenius relationships can be solved by using Table 3.1 in Jaeger with the linear and parabolic diffusivity constants and activation energies for wet and dry oxidation of $\langle 100 \rangle$. With these values, the calculated Deal-Grove constants assuming the field oxidation is a wet process done for 130 minutes at 1000°C, the gate oxidation is a dry process at 50 minutes and 1100°C, and the intermediate oxidation is a dry process for 25 minutes at 1100°C.

	B (μm^2/hr)	**A (μm)**
Field (Wet 1000°C)	0.3005	0.4046
Gate (Dry 1100°C)	0.0236	0.1395
Intermediate (Dry 1100°C)	0.0236	0.1395

Table 1: Deal-Grove constants at each oxidation step

By substituting in the Deal-Grove constants into the Deal-Grove quadratic model, we can solve for the thickness

$$X_o^2 + AX_o - Bt = 0 \implies X_o = \frac{-A + \sqrt{A^2 + 4Bt}}{2}$$

The field oxidation was done for 130 minutes at, the gate oxidation was done for 50 minutes and the intermediate oxidation was done for 25 minutes at 1150°C. These values are found in Table 2.

Thickness	**Value**
Field oxide (nm)	629.59
Gate oxide (nm)	86.85
Intermediate oxide (nm)	51.47

Table 2: Oxide thickness at each oxidation step

From a quick glance, these values do match our experimental oxide thickness and do make intuitive sense since the gate and intermediate oxides are much thinner since they underwent dry oxidation which is a much slower process.

3.2 Dopants

To calculate the distribution of dopants vs. wafer depth in the n-doped areas of the final wafer, we need to take into account the three initial sources of dopant atoms; a uniform boron doping, a boron ion implant, and the phosphorus diffusion. Firstly, we can find the background doping using the wafer resistivity. The process manual states that the starting wafer was a 3" uniformly doped p-type substrate with a resistivity of $0.14 - 0.16\ \Omega \cdot \text{cm}$. Using Jaeger Figure 4.8 and taking $\rho = 0.15\ \Omega \cdot \text{cm}$, we find that the doping concentration is

$$p \approx 2 \times 10^{16}\ \text{atoms/cm}^3$$

Since this is a background concentration or can be treated as spatially independent, we can write our background doping concentration as a function of x

$$p_{\text{background}}(x) = 2 \times 10^{16}\ \text{atoms/cm}^3$$

Ion implantation produces a Gaussian dopant distribution below the surface of silicon that is characterized by the projected range R_p, the peak configuration N_p and the straggle ΔR_p. These will allow us to determine what our median depth, peak height, and σ value is. Below is Jaeger Figure 5.2 which illustrates this

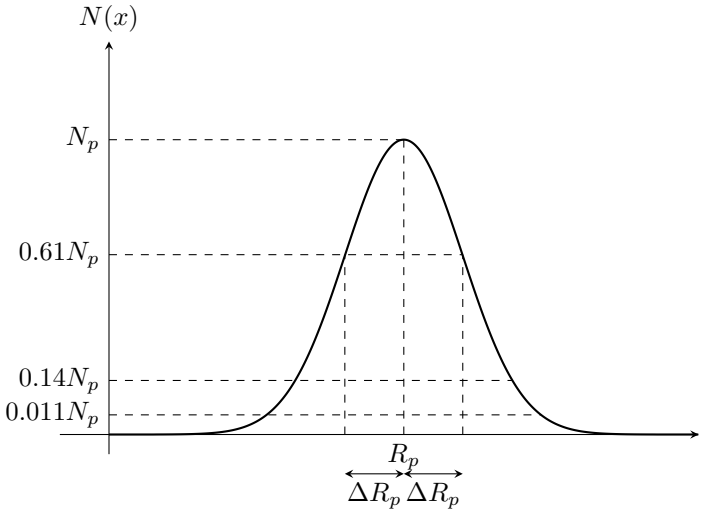


Figure 1: Jaeger 5.2 Gaussian impurity profile from ion implantation.

From the process manual, it is known that a blanket implant of 6.0×10^{12} cm^2 B11 ions were implanted at $E_A = 60$ keV. Firstly, using Jaeger Figures 5.3a and 5.3b (shown below in Figure 2 and 3), we can find the projected range, R_p, and straggle, ΔR_p, using this implant acceleration energy to get

$$R_p = 0.2\mu m,\ \Delta R_p = 0.06\mu m$$

As an ion enters the surface of the wafer and it collides with the atoms in the lattice and reacts with the electrons in the crystal. This is a statistical process and thus it can be approximated as a Gaussian distribution

$$N(x) = N_p \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right]$$

The area under the impurity distribution curve is the implanted dose Q and it can be simplified if the implant completely contained within the silicon, the dose is equal

$$Q = \int_0^\infty N(x)dx = \sqrt{2\pi} N_p \Delta R_p \implies N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p}$$

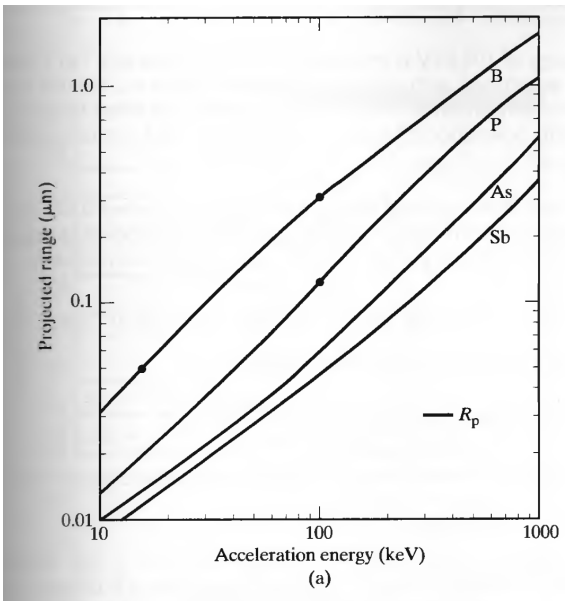


Figure 2: Jaeger 5.3a Projected range R_p for boron

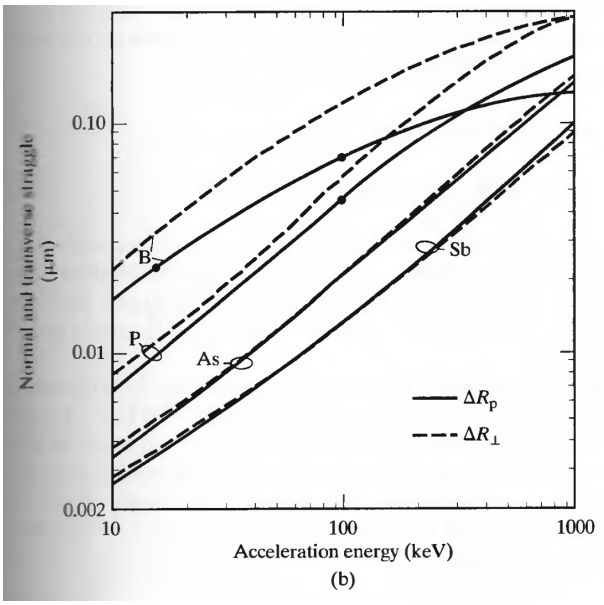


Figure 3: Jaeger 5.3b Vertical ΔR_p and transverse $\Delta R_\perp$ for boron

The process manual states the dosage $Q = 6.0 \times 10^{12}$ cm^2, so plugging this into the above equations yields the initial peak

$$N_p = \frac{Q}{\sqrt{2\pi}\Delta R_p} = \frac{6 \times 10^{12}\text{cm}^{-2}}{\sqrt{2\pi} \times 6 \times 10^{-6}\text{cm}} = 3.99 \times 10^{17}\text{cm}^{-3}$$

During oxidation and the phosphorus diffusion cycles, the implanted boron profile undergoes thermally activated diffusion which broadens the original Gaussian given by $N(x)$. The relevant thermal steps for our process are given as follows

- Field oxidation: 1000°C for 130 minutes.
- Gate oxidation: 1100°C for 60 minutes.
- Doping with P509 spin on dopant: 1100°C for 5 minutes.
- Drive in/intermediate oxide: 1100°C for 25 minutes.

For each of the four thermal steps above, the boron diffusivity D is found using the Arrhenius relationship

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right)$$

For each temperature, to find D we turn to Jaeger Table 4.1, where we find that the element specific diffusion constant for Boron is $D_0 = 10.5$ cm$^2/s$ with an activation energy of $E_A = 3.69$ eV. Below are the values of D at each thermal step

$$D_{\text{field}} = 2.596 \times 10^{-14}\ \text{cm}^2/s,\ D_{\text{gate}} = D_{\text{doping}} = D_{\text{drive-in}} = 3.006 \times 10^{-13}\ \text{cm}^2/s$$

Nowe, we can calculate the new Gaussian ion implantation profile after all thermal cycles using the four values of D from above. Note that thermal cycles accumulate linearly such that $Dt_{\text{eff}} = \sum D_i t_i$

$$C(x,t)\frac{Q}{\sqrt{2\pi(\Delta R_p^2 + 2Dt_{\text{eff}})}} \exp\left(\frac{(x-R_p)^2}{2(\Delta R_p^2 + 2Dt)}\right)$$

To model the boron spread, we note that the initial straggle is $\Delta R_p = 0.06\mu m$ and that taking a convolution of the Gaussian and adding those variances gives a new expression for the straggle at each step

$$\Delta R_p = \sqrt{\Delta R_p^2 + 2\sum_i D_i t_i}$$

$$\begin{aligned}
\Delta R_{p,\text{field}} &= \sqrt{(6\times10^{-6}\text{cm})^2 + 2(7800s)(2.596\times10^{-14}\ \text{cm}^2/s)} \\
&= 0.201\mu m \\
\Delta R_{p,\text{gate}} &= \sqrt{(2.01\times10^{-5}\text{cm})^2 + 2(3600s)(3.006\times10^{-13}\ \text{cm}^2/s)} \\
&= 0.507\mu m \\
\Delta R_{p,\text{inter}} &= \sqrt{(5.07\times10^{-5}\text{cm})^2 + 2(1500s)(3.006\times10^{-13}\ \text{cm}^2/s)} \\
&= 0.589\mu m = \Delta R_{\text{final}}
\end{aligned}$$

Then, we can substitute these values into the dosage equation to give us the peak boron dopant concentration

$$N_{p,\text{final}} = \frac{Q}{\sqrt{2\pi}\cdot\Delta R_{p,\text{final}}} = \frac{6\times10^{12}\text{cm}^{-2}}{\sqrt{2\pi}\cdot0.589\mu m} = 4.06\times10^{16}\text{atoms/cm}^3$$

Note that the depth of the boron peak concentration is assumed to be the average depth of the original ion implantation which was computed via the ion implant energy and Jaeger Figure 5.4 ignoring any effects from the oxide and is hence $R_p = 0.2\mu m$. Therefore, the boron concentration as a function of depth is

$$N_{\text{boron}}(x) = 4.06\times10^{16}\text{atoms/cm}^3\exp\left(\frac{-(x-0.2\mu m)}{2(0.5056\mu m)^2}\right)$$

Next, we need to calculate the first n-type doping step with phosphorus diffusion under constant-source conditions. This process to get our dopants into our silicon means that the phosphorus-doped SOG provides an effectively unlimited dopant supply, the surface concentration stays fixed at the solid-solubility limit, and the rate of doping is controlled entirely by diffusion within the silicon rather than by the availability of dopant. This is modeled in Jaeger Figure 4.2. Mathematically,

$$N(x,t) = N_0\text{erfc}\left(\frac{x}{2\sqrt{Dt}}\right)$$

To determine the value of N_0, we take the solid solubility limit of phosphorus in Si at this temperature. Using Jaeger Figure 4.6 on the next page, and using a temperature of 1100°C, we find our solubility/impurity concentration N_0 to be 1.5×10^{21} atoms/cm^3. We can use this to find the source-limited profile. The dose after diffusion of phosphorus can be found using

$$Q_{\text{phosphorus}} = 2N_0\sqrt{Dt_1/\pi} = 2(1.5\times10^{21}\text{atoms/cm}^3)\sqrt{(3.006\times10^{-13}\text{cm}^2/s)(1500s)/\pi} = 3.59\times10^{16}\text{cm}^{-2}$$

And then applying this dosage to the Gaussian, we can find the concentration distribution of phosphorus in Si as a function of depth

$$N_{\text{phosphorus}}(x,t) = 1.5\times10^{21}\text{atoms/cm}^3\text{erfc}\left(\frac{x}{0.3\mu m}\right)$$

The depth of phosphorus at the peak concentration is taken to be $0\mu m$ since it is at the surface and we ignore the effects from dopant redistribution into the oxide.

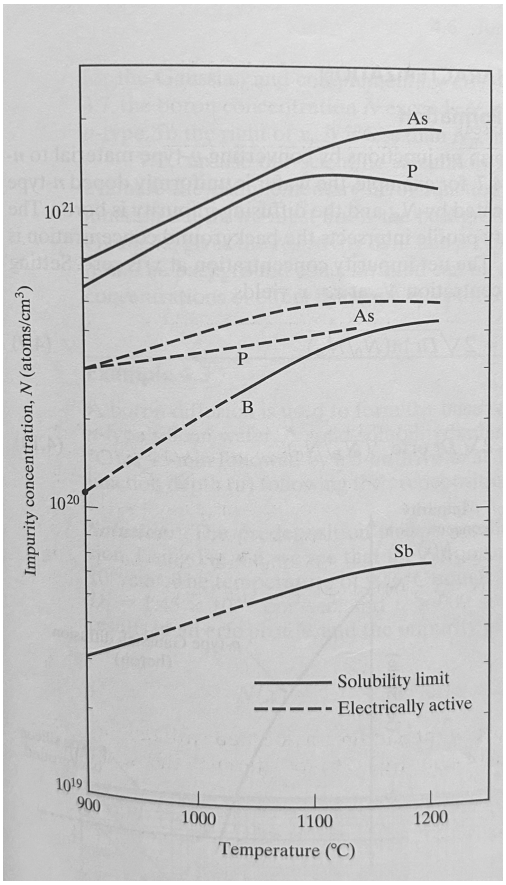


Figure 4: Jaeger 4.6 Solid-solubility

The junction depth, x_j, is the point at which the concentration of dopants equals the background impurity concentration i.e. $N_n = N_p$. Note that the hole doping concentration is the background Boron dopeing plus the Gaussian doping after all the thermal diffusion. Thus, x_j is found by solving

$$1.5 \times 10^{21} \operatorname{erfc}\left(\frac{x_j}{0.3\ \mu\text{m}}\right) = 2 \times 10^{16} + 4.06 \times 10^{16} \exp\left[-\frac{(x_j - 0.2\ \mu\text{m})^2}{2(0.589\ \mu\text{m})^2}\right]$$

This equation is solved numerically. Evaluating both sides over the range 0.8–1.0 μm shows that the donor and acceptor concentrations intersect at approximately

$$x_j \approx 0.9\ \mu\text{m}$$

The resistivity of a $\langle 100 \rangle$ Si is given by its intrinsic carrier concentrations and mobilities

$$R_s = \frac{\rho}{x_j}, \text{ where } \rho = \frac{1}{q(\mu_n n + \mu_p p)}$$

For the sheet resistance in the n-section, we can use the integral relation

$$R_s = \left(\int_0^{x_j} q\mu_n N(x) dx\right)^{-1}$$

We use this integral form because the doping concentration is a function of depth, and therefore the resistivity will be as well. Using the phosphorus concentration profile for $N_D(x)$, we have

$$R_s = \left(q\mu_n N_0 \int_0^{0.9\mu m} \operatorname{erfc}\left(\frac{x}{0.3\mu m}\right)\right)^{-1}$$

Using this chart below[1] we can find the carrier mobilities in silicon as a function of the doping concentration.

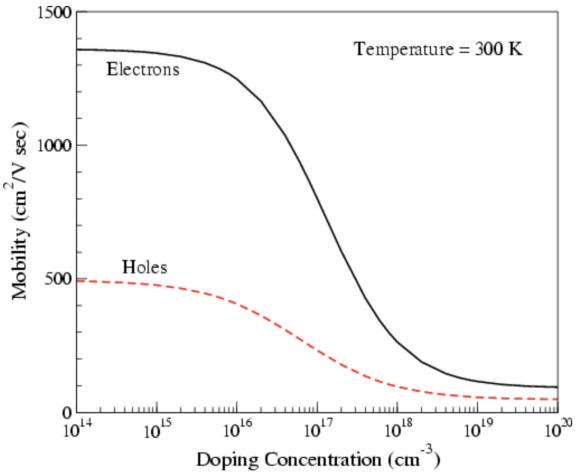


Figure 5: Room temperature carrier mobilities in silicon as a function of the doping concentration.

With $q = 1.6 \times 10^{-19}$C, $\mu_n = 60\text{cm}^2/s$ from the Masetti model, and $N_0 = 1.5 \times 10^{21}\text{atoms/cm}^3$, we use MATLAB to numerically evaluate the integral and we get

$$R_{s,n} = 4.10\Omega/\square$$

For the sheet resistance in the p-section, the background doping dominates the sheet resistance. This is because the entire thickness of the wafer can conduct current and thus no integral relation is needed. So, we use the bulk resistivity of the starting wafer and divide by the thickness

$$R_{s,p} = \frac{\rho}{t} = \frac{15\Omega \cdot cm}{0.038cm} = 395\Omega/\square$$

The lateral diffusion of phosphorus can be found using the commmon rule of thumb, that is

$$x_{\text{lat}} = 0.7 \times x_j = 0.7 \times 0.9\mu m = 0.63\mu m$$

3.3 Plots

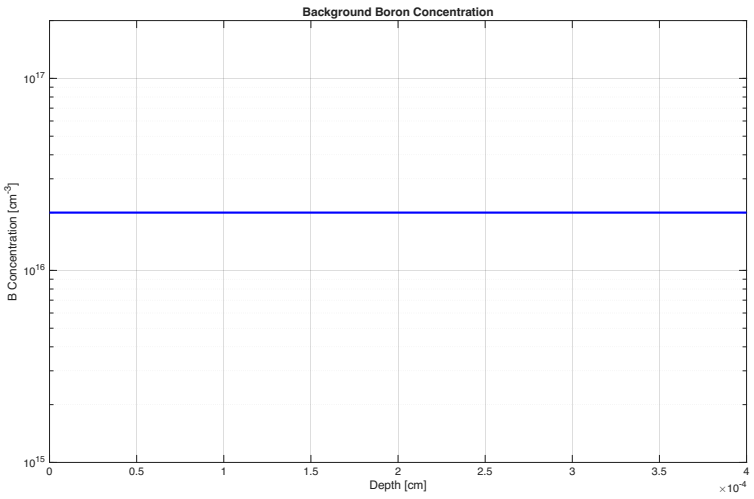


Figure 6: Background Boron Concentration

[1] Institut für Mikroelektronik der TU Wien

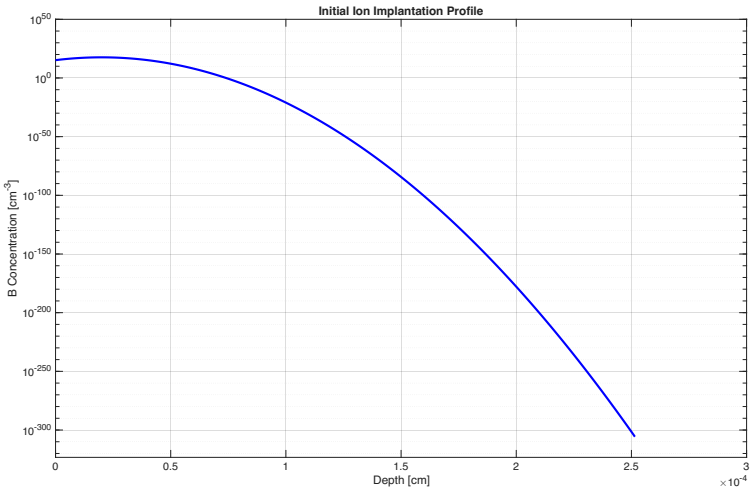


Figure 7: Initial Ion Implantation Profile

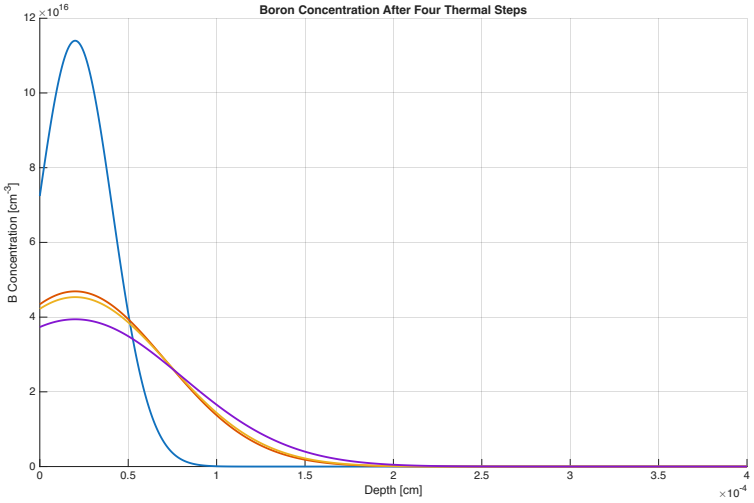


Figure 8: Boron Concentration After Four Thermal Steps

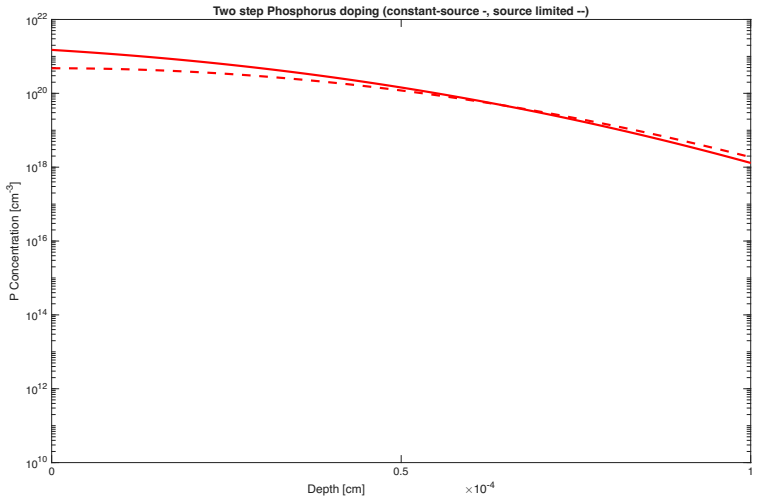


Figure 9: Two step Phosphorus doping

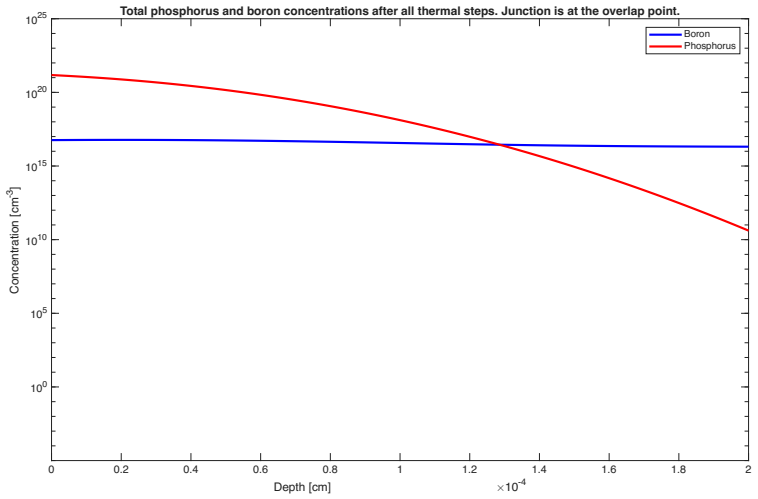


Figure 10: Total phosphorus and boron concentrations after all thermal steps.

3.4 Aluminum

Assuming the ideal thickness of evaporated aluminum is $t = 100$ nm, we can compute the sheet resistance of this film. The bulk resistivity, ρ, of aluminum (Al) at 20°C is given as $\rho = 2.65 \times 10^{-8}\,\Omega \cdot \mathrm{m}$[2]. Recall that the sheet resistance R is defined by

$$R_s = \frac{\rho}{t} = \frac{2.65 \times 10^{-8}\,\Omega \cdot \mathrm{m}}{100\ \mathrm{nm}} = \frac{2.65 \times 10^{-8}\,\Omega \cdot \mathrm{m}}{10^{-7}\ \mathrm{m}} = 0.265\Omega/\square$$

Therefore, the final sheet resistance for a 100 nm film of aluminum is

$$\boxed{R_s = 0.265\Omega/\square}$$

3.5 Doping Summary

[2] Georgia State Univerity HyperPhysics Concepts

All the theoretical calculations results from doping is summarized as follows:

Parameter	Value
Boron peak concentration (atoms/cm^3)	4.06 x 10^{16}
Depth of boron peak concentration (µm)	0.2
Phosphorus peak concentration (atoms/cm^3)	10^{21}
Depth of phosphorus peak concentration (µm)	0
Junction depth (µm)	0.9
Sheet resistance of areas with no phosphorus doping (Ω/square)	395
Sheet resistance of areas with phosphorus doping (Ω/square)	4.10
Lateral diffusion of phosphorus (µm)	0.63

PART 4: Process Deviations

Process Deviations

The ACTV, POLY, CONT, and METL overetching could be caused by overexposure and overdevelopment during the wet etching stage. Overetching is preferred to ensure that the etching patterns are completely transferred to the silicon wafer.

Lithography step	Average overetch from lithography (μm)	Average overetch from wet etching (μm)
ACTV	0.32	0.4425
POLY	0.5475	1.215
CONT	0.27	0.6325
METL	0.305	0.8325

Misalignment

We did not measure the CONT-POLY mask in our lab section. The misalignment can be attributed to human error in aligning the mask while operating the mask aligner. For example, while the mask can appear to be aligned under the microscope, the mask could be slightly skewed.

Parameter	X misalignment (μm)	Y misalignment (μm)
ACTV-POLY	0.039	0.058
ACTV-CONT	0.058	0.108
CONT-METL	0.09	0.02

Oxide Growth

Doped silicon grows oxide more slowly, which means that it is difficult to control the rate of oxidation besides using the Deal-Grove model. For the dry oxidation steps, the discrepancy can be attributed to the wafer position in the furnace, which has an uneven temperature distribution. For the wet oxidation steps, the discrepancy can be attributed to one of many parameters, such as the gas flow rate, the water vapor

concentration, and the amount of time that the wafer is placed in the oxidation furnace.

Oxidation step	Theoretical thickness (nm)	Measured thickness (nm)
Field oxidation	629.59	620
Gate oxidation	86.85	109.1
Intermediate oxidation	51.47	67.3

Doping

We did not measure the sheet resistance before phosphorus doping in our lab section. We measured a higher sheet resistance after phosphorus doping than the theoretical value. There could be discrepancies with the dopant diffusion depth across the wafer in different regions caused by contaminants and surface damage. The discrepancies can also be caused by varying phosphorus activation in the dopant drive-in furnace step.

Doping profile	Theoretical value (Ω/square)	Measured value (Ω/square)
Sheet resistance before phosphorus doping	395	N/A
Sheet resistance after phosphorus doping	4.10	5.93

Aluminum

The measured value is lower than the expected value, which could mean that there is more aluminum deposited in the areas that are measured compared to the theoretical value. Surface contamination can cause varied film thickness across the wafer.

Aluminum	Theoretical value (Ω/square)	Measured value (Ω/square)
Sheet resistance	0.265	0.124

PART 5: Questions

5.1 Questions

1. We do lithography steps under yellow light only. What would happen if we exposed the wafer to white light or sunlight before development? What about after development? Would red light damage your process?

   Solution

   In lithography, we use yellow light because photoresist is sensitive to UV and short wavelength blue light. If the wafer is exposed to white light or sunlight before development, those wavelengths will keep exposing the resist and destroy the pattern you want to print. After development, the pattern is mostly fixed, so white light won't cause major damage, although very strong UV could still degrade the resist slightly. Red light is completely safe, since its wavelength is far from the range that activates photoresist chemistry.

2. Describe our photoresist. Do we use positive or negative photoresist? I-line or G-line? What do I-line and G-line mean? Briefly describe how the photoresist responds to spinning, UV light exposure, and development.

   Solution

   We use I-line positive photoresist, specifically the MIR 701 photoresist. G-line photoresist responds to around 436 nm and I-line responds to around 365 nm wavelengths of light respectively. The photoresist responds to spinning by spreading itself across the wafer radially as it spins on the 3000 RPM spinner. Since the photoresist is a positive photoresist, exposed photoresist with UV light exposure is weakened.

   Photoresist developer is used to remove areas of positive photoresist that is exposed, which means that exposed photoresist will be removed and reveal the underlying layer. The underlying layer can then be etched away with HF or deposited with metal for the metal interconnects.

3. What are the purposes of the 110°C pre-photoresist bake, HMDS, softbake, post-exposure bake, and hard bake?

   Solution

   The 110°C pre-photoresist bake removes moisture from the wafer to improve resist adhesion. HMDS further primes the surface by making it hydrophobic so the photoresist bonds properly. After coating, the softbake step drives off excess solvents to stabilize the resist film and prepare it for uniform exposure. After UV exposure, the post-exposure bake helps complete the photochemical reactions. Finally, the hard bake strengthens and creates crosslinks in the developed resist to make it durable for the following processing steps.

4. What is the difference between wet and dry oxidation, and why do we choose one for field oxidation and the other for gate oxidation?

   Solution

   Wet and dry oxidation both grow SiO_2 on silicon, but they differ in speed and quality. Wet oxidation uses water vapor to supply the oxygen to the silicon and grows oxide much faster, producing a thicker but slightly lower-quality film with more impurities and a looser structure. Dry oxidation uses pure oxygen and grows oxide more slowly, but the resulting layer is denser and cleaner with less roughness and defects.
   Because of this, we use wet oxidation for field oxide—where we need a thick insulating layer to isolate devices and small defects don't matter. In contrast, we use dry oxidation for the gate oxide, because the gate dielectric has to be thin and uniform to ensure that the transistor behaves as expected.

5. Why is it important to clean the wafer in HF immediately before depositing spin-on glass? Also, why do wafers need to be cleaned well before furnace steps?

Solution

It's important to clean the wafer in HF immediately before depositing spin-on glass because HF removes the native oxide and leaves a clean hydrophobic silicon surface. Native oxide regrows within minutes in air, and if it's present, the spin-on glass will not adhere uniformly leading to poor coverage, film peeling, and other defects.

Wafers must also be cleaned thoroughly before any furnace step because high temperatures can cause contaminants, such as other metals and organics, to diffuse into the silicon, which creates non-uniform oxidation. Clean wafers ensures uniform thermal reactions, predictable oxide growth, and prevents contamination from spreading throughout the furnace tube.

6. What is the difference between 5:1 HF and 10:1 HF, and why do we need both for different steps? Also, the HF we use in lab is actually buffered HF (a mixture of pure HF and NH_4F); why is this?

Solution

The difference between 5:1 HF and 10:1 HF comes from their NH_4:HF ratios, which controls the etch rate of the solution based on their HF concentration. A 5:1 mixture etches SiO_2 faster, which is useful for steps that remove oxide quickly or open features with less concern about over-etching. In contrast, 10:1 HF is more dilute and etches slower, which is important for delicate steps such as removing only a thin native oxide layer before deposition or whenever dimensional control is critical.

We don't use pure HF in our lab. Instead, we use buffered HF (HF mixed with NH_4F), because the ammonium fluoride acts as a reservoir of fluoride ions that maintains a nearly constant concentration of the reactive species. This buffering prevents rapid depletion of HF and stabilizes the pH, which improves uniformity of etching rate across the wafer and increases selectivity.

7. When designing a new microfabrication process, how do you know how long etch steps should be? Provide at least two different methods.

Solution

When designing a new microfabrication process, we should determine how long etch steps are by using both predictive calculations and empirical calibration. First, we can look up etch rate data for a specific material from vendor datasheets, manuals, and literature. We can estimate the time by dividing the film thickness by the stated nominal etch rate, and we can get a slight overetch by adding a small margin (for example, 10-20%)

Second, we can calibrate by etching control wafers with known thicknesses for different time durations. Then, we can measure the remaining thickness with multiple methods, such as ellipsometry, profilometry, or reflectometry, and then plot the thickness over time to get an accurate etch rate.

8. Why does the aluminum evaporator have two vacuum pumps: a roughing pump and turbopump? Describe how they are used.

Solution

The aluminum evaporator uses two vacuum pumps, a roughing pump and a turbopump, because each operates best in a different pressure range. Both are needed to reach the high vacuum required for metal evaporation.

The roughing pump handles the first stage. It removes most of the air from the chamber and brings the pressure down from atmospheric pressure to the medium vacuum range (around 10^{-2}—10^{-3} Torr). However, it cannot reach the very low pressures needed for high-quality evaporation.

Once the chamber is at very low pressures, the turbomolecular pump takes over to remove the remaining gas particles. Turbopumps only work effectively at low pressures, and they further reduce the chamber pressure to the high- or ultra-high-vacuum range (10^{-6} Torr or better). At this vacuum level, metal evaporates cleanly, without oxidation or scattering, producing a uniform, high-purity aluminum film.

9. Please describe how our following metrology tools work and what they are useful for: the optical microscope, four-point probe, and Nanospec thin film measurement tool.

Solution

An optical microscope uses visible light and a system of lenses to magnify features on the wafer surface, allowing inspection of photoresist patterns, defects, alignment marks, etch quality, and overall pattern fidelity. It is useful for quickly checking lithography results, verifying feature dimensions at the micron scale, and identifying particulate contamination or pattern failures without damaging the sample.
The four-point probe measures the sheet resistance of conductive thin films by sourcing current through the outer two probes and measuring the voltage drop across the inner two. Because this geometry minimizes contact resistance, it provides an accurate measurement of film resistivity and uniformity, which is needed for characterizing doped silicon, metals, or semiconductor layers after deposition, implantation, or annealing.

The Nanospec thin-film measurement tool determines film thickness using optical reflectometry. It shines monochromatic light onto the wafer, measures the intensity of light reflected back, and analyzes the interference pattern created by reflections from the top and bottom surfaces of the film. By matching the measured spectrum to known models of material optical properties, the tool can extract film thickness with nanometer-scale precision. Nanospec is therefore used to monitor oxide, nitride, or polymer thicknesses before and after etching or deposition steps to ensure proper process control throughout microfabrication.

10. For two different processes, please explain how they could be replaced with a different process you learned about in lecture, and the pros and cons of doing so (e.g., replacing spin-on glass with ion implantation).

Solution

We can replace wet oxide etch with HF with reactive ion etching. The pro is that we will have improved alignment, better critical dimension control, and less over-etching. The con is that the plasma can unintentionally damage other parts of the wafer because of lower selectivity. Reactive-ion etching also needs expensive equipment.

Another example is replacing thermal diffusion doping with ion implantation. Traditional diffusion relies on high-temperature furnace steps to drive dopants into silicon, but this process lacks precision and can create deeper junctions than desired. Ion implantation allows us to accurately control dopant dose and depth. However, implantation damages the crystal lattice structure and requires annealing to repair the structive and activate the dopants after. Implant tools are also more expensive.